DETAILED ACTION

Applicant's amendment received on 3/25/08 has been entered.

Response to Amendment

In light of the newly discovered art arguments with respect to claims 1, 3-8, 11-13, 15-18, 20-30 and 32-34 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1, 3-8, 11-13, 15-18, 20-30 and 32-34 have been examined.

Claim Objections

1. Claims 1 and 25 are objected because the term "choatic" (claim 1, line15) should read "chaotic" and the term "witin" (claim 25 in line 6, page 11) should read "within".

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1, 3-8, 11-13, 15-18, 20-30 and 32-34 are rejected under 35 U.S.C. 101 because the claim language as cited is essentially directed towards an algorithm. None of the claim language suggests a hardware implementation of the claimed steps and even claim 15, although directed towards "a system" that comprises "a

transmitter", "a receiver", "a generator", etc. could be simply implemented in software as program modules.

Amending the claim language indicating the use of computer hardware with a proper support from the specification would overcome the 35 U.S.C. 101 rejection.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 3-8, 11-13, 15-18, 20-30 and 32-34 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-29 of copending application No. 10/614260. Claims 1, 3-8, 11-13, 15-18, 20-30 and 32-34 of the instant application anticipate and/or are obvious variation of claimed subject matter of the application No. 10/614260.

See the example below:

Claim 1 and 3, application 10/614260	Instant application
1. A method for transmitting and receiving a digital message having N digits, each of said N digits having any one of M values, in a system wherein each of said M values k	1. A method for transmitting and receiving a digital message having N digits, each of said N digits having any one of M values, in a system wherein each of said M values k
o corresponds with a kth-second chaotic signal generator associating with a kth-second chaotic algorithm; and	o corresponds with a kth-chaotic signal generator having chaotic characteristic value associating with a chaotic algorithm; and
o is transmitted within a bit period as a chaotic signal comprising a first chaotic signal and a second chaotic signal, the bit period being divided into a first portion and a second portion	o is transmitted within a bit period
including the steps of:	including the steps of:
•generating the first chaotic signal from a first chaotic signal generator by a first chaotic algorithm, and transmitting the first chaotic signal in the first portion of the bit period;	
• selecting the corresponding kth-second chaotic signal generator;	(i) selecting the corresponding k-th second chaotic signal generator;
• feeding the first chaotic signal to the kth-second chaotic signal generator to generate the second chaotic signal, and	(ii) generating a chaotic signal by the corresponding kth-chaotic signal generator.;.
transmitting the second chaotic signal in the second portion of the bit period; and	(iii) transmitting said chaotic signal; and
• receiving the first and second chaotic signals at a receiver storing a demodulating algorithm, and demodulating the chaotic signals to generate the transmitted value k wherein the first and second chaotic signals are sent at any order	(iv) receiving the chaotic signal at a receiver storing the chaotic characteristic values of all chaotic signal generators used to transmit said message and a demodulating algorithm, and demodulating the chaotic signal to generate the transmitted value k,
Claim 3.	
<u>The method as claimed in Claim 1</u>, wherein the chaotic signal is demodulated by the demodulating algorithm by the steps of	said demodulation of the chaotic signal by the demodulating algorithm including the steps of:

• separating the first and second chaotic signals received at the receiver;	
• transforming the first signal received at the receiver according to the second chaotic algorithm for each of the second chaotic signal generators to generate a plurality of transformed chaotic signals;	(i) evaluating the chaotic characteristic value of the received chaotic signal;
• matching the second chaotic signal with the plurality of transformed first chaotic signals; and	(ii) matching the evaluated chaotic characteristic value of the received chaotic signal with the chaotic characteristic values stored in the receiver; and
• assigning the transmitted value according to the closest match between the second chaotic signal and the plurality of transformed first chaotic signals	(iii) assigning the transmitted value k by reference to the closest match between the evaluated chaotic characteristic value and the stored chaotic characteristics values

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, 18 and 20 are rejected under 35 U.S.C. 102(b) based as being anticipated by IEEE (Andrey Kisel, Herve Dedieu and Thomas Schimming, "Maximum Likelihood Approaches for Noncoherent Communications with Chaotic Carriers", IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications, Vol. 48, No. 5, May 2001).

As per claims 1 and 18, IEEE discloses a method for transmitting and receiving a digital message having N digits, each of the N digits having any one of M values in a system, wherein each of the M values k corresponds with a kth-chaotic signal generator having chaotic characteristic value associating with a chaotic algorithm and is transmitted within a bit period including the steps of selecting the corresponding kth-chaotic signal generator, generating a chaotic signal by the corresponding kth-chaotic signal generator and transmitting the chaotic signal (see modulation in Fig. 7 and associated text, for example. Note that although for purpose of simplicity the examiner discusses CSK model disclosed in Fig. 7, Fig. 9 and differential chaos shift keying DCSK, which is a variation of the CSK model also applies to claimed limitations), receiving the chaotic signal at a receiver storing the chaotic characteristic values of all chaotic signal generators used to transmit the message (demodulation in Fig. 7 and 8 and associated text, for example). IEEE discloses that the demodulation of the chaotic signal evaluating the chaotic characteristic value of the received chaotic signal, matching the evaluated chaotic characteristic value of the received chaotic signal with the chaotic characteristic values stored in the receiver and assigning the transmitted value k by reference to the closest match between the evaluated chaotic characteristic value and the stored chaotic characteristics values (IEEE, pg. 539, for example).

5. As per claims 3, 20, the chaotic signal produced by chaotic generators disclosed by IEEE inherently includes a series of numbers. Each number is transmitted within the

bit period (see Fig. 7 and associated text, for example), and on pg. 538 (and 539) IEEE discloses generators using algorithms.

Claim Rejections - 35 USC § 102 or 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6 and 23 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over IEEE (Andrey Kisel, Herve Dedieu and Thomas Schimming, "Maximum Likelihood Approaches for Noncoherent Communications with Chaotic Carriers", IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications, Vol. 48, No. 5, May 2001).
   IEEE discloses a method for transmitting and receiving a digital message having N digits, each of said N digits having any one of M values as discussed above.
7. Although IEEE does not explicitly disclose M equal to 2 with each digit having a value of either 0 or 1, the limitation, if not inherent, is at least implicit. M equal to 2 in IEEE's invention and computers operate on binary values: 0s and 1s. Thus, in order to represent these two values in a computer system, it would have been implicit, if not inherent to utilize these two different values: 0 and 1.
8. Claims 7 and 24 are rejected under 35 U.S.C. 103(a) as obvious over IEEE (Andrey Kisel, Herve Dedieu and Thomas Schimming, "Maximum Likelihood Approaches for

Noncoherent Communications with Chaotic Carriers", IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications, Vol. 48, No. 5, May 2001). IEEE teaches modulation and demodulation performing the steps discussed above.

9. Although, IEEE does not teach that the chaotic algorithm utilizing the steps is $y=m[0.5-2|x|]$, an ordinary artisan would readily recognize that a particulars of the algorithm would not affect the functionality of the claimed method. Furthermore, it would have been obvious to an ordinary artisan to try different algorithms given the benefit of finding the most efficient operation of the system.

10. Claims 4-5, 8, 11-13, 15-17, 21-22, 25 and 28-30, 32-34 are rejected under 35 U.S.C. 103(a) as obvious over IEEE (Andrey Kisel, Herve Dedieu and Thomas Schimming, "Maximum Likelihood Approaches for Noncoherent Communications with Chaotic Carriers", IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications, Vol. 48, No. 5, May 2001) in view of Umeno (USPN 6661831) and Menezes et al. (Alfred J. Menezes, Paul C. van Oorschot, Scott A. Vanstone, "Handbook of applied cryptography", 1997, ISBN: 0849385237). IEEE teaches generating the chaotic signal as discussed above.

11. Additionally, as per claims 5, 32 and 34, IEEE discloses repeating the step of pairing the first two numbers of the chaotic signal received by the receiver to form a first plot on a two-dimensional plane and matching the evaluated chaotic value of the return map with the stored chaotic values (Fig. 8 and 10 and associated text, for example).

12. As per claims 4, 8, 13, 21, 25 and 30, IEEE does not explicitly disclose inputting a random number to the chaotic algorithm to generate a first chaotic number. Umeno

discloses inputting a random number to generate a first chaotic number (Umeno, col. 5 lines 64-67). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to input a random number to generate a first chaotic number in IEEE's invention given the benefit of increased security.

13. IEEE in view of Umeno does not disclose inputting the first chaotic number to the chaotic algorithm to generate a second chaotic number and repeating the step of using the second chaotic number as the first chaotic number until all number to be transmitted within the bit period are generated. However, the examiner points out that this technique (generating a second chaotic number and repeating the step of using the second chaotic number as a first chaotic number until all numbers to be transmitted are generated) is old, well known and frequently used in the art of computer security (see Menezes, pg. 229, Fig. 7.1 d, for example). It would have been obvious to an ordinary artisan to generate a second chaotic number and repeating the step of using the second chaotic number as the first chaotic number until all number to be transmitted within the bit period are generated given the benefit of efficient mechanism or additional ambiguity.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter Poltorak whose telephone number is (571) 272-3840. The examiner can normally be reached Monday through Thursday from 9:00 a.m. to 4:00 p.m. and alternate Fridays from 9:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on (571) 272-3811. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Peter Poltorak/

Examiner, Art Unit 2134

/Kambiz Zand/

Supervisory Patent Examiner, Art Unit 2134